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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/742,916	12/23/2003	Linus Albert Fetter	37310-000107/US	7346

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EXAMINER	
ROSENAU, DEREK JOHN	

ART UNIT	PAPER NUMBER
2834	

DATE MAILED: 12/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/742,916	FETTER ET AL.
	Examiner	Art Unit
	Derek J. Rosenau	2834

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "215" has been used to designate both an input port and a protected metal layer. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "200" has been used to designate both a T-cell building block and a TFR. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: the continuity date should be updated to reflect that application 09/698175 has issued as 6675450.

Appropriate correction is required.

Claim Objections

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 12 recites the limitation "said piezoelectric material" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. Claim 10 refers to a piezoelectric layer.

6. Claim 12 recites the limitation "said conductive films" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim. Claim 10 refers to conductive layers.

7. Claim 1 is objected to because of the following informalities: the phrase “an thin film resonator” is grammatically incorrect. This should be replaced with “A thin film resonator.” Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-6 and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Kaitila et al. (US 6812619).

10. With respect to claim 1, Kaitila et al. discloses a thin film resonator (TFR) device, comprising: a substrate (Fig 3, item 200) having an etch-resistant thin film thereon (Fig 3, item 130); and a piezoelectric material layer (Fig 3, item 100) formed between first and second conductors (Fig 3, items 110 and 120), said first conductor contacting said etch-resistant thin film, the etch-resistant thin film and substrate configured as a suspended membrane supporting said first and second conductors and said piezoelectric layer (Fig 3).

11. With respect to claim 2, Kaitila et al. discloses the TFR device of claim 1, wherein the etch resistant film acts as a barrier to allow removal of substantially all of said substrate to form a membrane that supports said piezoelectric layer and said first and second conductors (Fig 3).

12. With respect to claim 3, Kaitila et al. discloses the TFR device of claim 1, wherein said piezoelectric material is a material selected from the group consisting of AlN, SiN, and ZnO (column 2, lines 13-16).

13. With respect to claim 4, Kaitila et al. discloses the TFR device of claim 1, wherein said first and second conductors are Al metal electrodes or other conductors (column 2, lines 21-25).

14. With respect to claim 5, Kaitila et al. discloses the TFR device of claim 1, wherein said substrate is formed of silicon, quartz, or glass (column 1, lines 61-63).

15. With respect to claim 6, Kaitila et al. discloses the TFR device of claim 1, wherein said substrate is essentially immune to effects of parasitic capacitance and inductance. While Kaitila et al. does not expressly state such immunity, the disclosed structure performs this function as the substrate has been removed below the conductors.

16. With respect to claim 10, Kaitila et al. discloses an electronic device, comprising: a substrate (Fig 3, item 200) having an etch-resistant thin film thereon (Fig 3, item 130); and a piezoelectric layer (Fig 3, item 100) formed between first and second conductor layers (Fig 3, items 110 and 120), the etch-resistant thin film forming a suspended membrane supporting the electronic device (Fig 3).

17. With respect to claim 11, Kaitila et al. discloses the device of claim 10, wherein the etch resistant thin film thereon acts as a barrier to allow removal of substantially all of said substrate to form the suspended membrane supporting said piezoelectric layer and conductor layers of the electronic device (Fig 3).

18. With respect to claim 12, Kaitila et al. discloses the device of claim 10, wherein said piezoelectric material is selected from a group consisting of AlN, SiN, and ZnO (column 2, lines 13-16); said conductive films are Al metal electrodes or other conductors (column 2, lines 21-25); and said substrate is formed of silicon, quartz, or glass (column 1, lines 61-63) and is essentially immune to the effects of parasitic capacitance and parasitic inductance. While Kaitila et al. does not expressly state such immunity, the disclosed structure performs this function as the substrate has been removed below the conductors.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 7-9, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaitila et al. (US 6812619) in view of Fischer et al. (US 5701032).

21. With respect to claim 7, Kaitila et al. discloses the TFR device of claim 1.

Kaitila et al. does not disclose expressly that the device further comprises a plurality of solder bumps that are applied to the ends of leads extending from said first and second conductors, wherein said leads are formed on a die that supports the TFR device.

Fischer et al. teaches a package for integrated circuits that utilizes solder bumps applied to the leads (column 10, lines 27-32), and that these leads are formed on a die that supports the integrated circuit device (column 2, lines 13-15).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the packaging arrangement of Fischer et al. with the TFR of Kaitila et al. for the benefit of obtaining an improved packaging design.

22. With respect to claim 8, the combination of Kaitila et al. and Fischer et al. disclose the TFR device of claim 7.

Kaitila et al. does not disclose expressly that the die is attached to a carrier intended for the device so that said solder bumps contact corresponding bonding leads on said carrier or package; or that the solder bumps are reflowed to effect electrical connection to the carrier or package.

Fischer et al. teaches a package for integrated circuits with solder bumps corresponding to bonding leads on the package (column 10, lines 27-32) and that the solder bumps are reflowed to effect electrical connection to the package (column 10, lines 47-49).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the packaging arrangement of Fischer et al. with the TFR of Kaitila et al. for the benefit of obtaining an improved packaging design.

23. With respect to claim 9, the combination of Kaitila et al. and Fischer et al. discloses the TFR device of claim 8.

Kaitila et al. does not disclose expressly that the carrier or package connected device is configured so that the effects of any residual parasitic capacitances and parasitic inductances are negated or limited.

Fischer et al. teaches a package for integrated circuits that is configured to limit parasitic capacitances and inductances (column 9, lines 16-19).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the parasitic capacitance and inductance reducing characteristics of Fischer et al. with the TFR device of Kaitila et al. for the benefit of eliminating unwanted capacitive and inductive effects.

24. With respect to claim 13, Kaitila et al. discloses the device of claim 10.

Kaitila et al. does not disclose expressly that a plurality of solder bumps are applied to ends of leads extending from said conductors, wherein said leads are formed on a die that supports the device.

Fischer et al. teaches a package for integrated circuits that utilizes solder bumps applied to the leads (column 10, lines 27-32), and that these leads are formed on a die that supports the integrated circuit device (column 2, lines 13-15).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the packaging arrangement of Fischer et al. with the TFR of Kaitila et al. for the benefit of obtaining an improved packaging design.

25. With respect to claim 14, Kaitila et al. discloses the device of claim 10.

Kaitila et al. does not disclose expressly that the die is attached to a package intended for the device so that said solder bumps contact corresponding leads on said

package; or that the solder bumps are reflowed to effect electrical connection to the package.

Fischer et al. teaches a package for integrated circuits with solder bumps corresponding to bonding leads on the package (column 10, lines 27-32) and that the solder bumps are reflowed to effect electrical connection to the package (column 10, lines 47-49).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the packaging arrangement of Fischer et al. with the TFR of Kaitila et al. for the benefit of obtaining an improved packaging design.

Conclusion

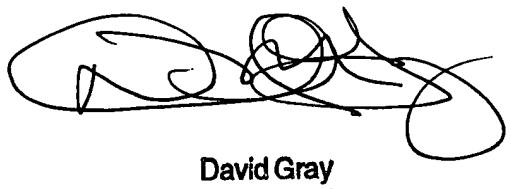
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Derek J. Rosenau whose telephone number is 571-272-8932. The examiner can normally be reached on Monday thru Friday 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Gray can be reached on 571-272-2119. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Derek J Rosenau
Examiner
Art Unit 2834

DJR
12/16/05



David Gray
Primary Examiner